Application No.: 09/539,966 Attorney Docket No.: EMC2-044PUS
(formerly 07072-101001)

REMARKS/ARGUMENTS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

It is noted that the Examiner did not consider an Information Disclosure Statement filed electronically on January 4, 2005. A copy is enclosed.

With regard to the provisional double patenting rejection, this issued will be addressed when allowable subject matter is found.

In reviewing the claims, it was noted that the term "messag*ing* network" and "message network" have been used interchangeably. In order for there to be consistency, the term "message network" was selected and therefore the term "messaging network" has been changed to "message network" throughout the claims.

The claims stand rejected under 35 USC 103(a) as being unpatentable over Martin et al. (U. S. Patent No. 5,214,768) in view of Gaskins (U. S. Patent No. 5,903,911).

It is Applicant's position, for reasons set forth in detail below that: (1) adding a global memory to Martin et al. would, contrary to the Examiner's assertion, reduce system bandwidth because such global memory is accessible by all directors and therefore would, with the Examiner's suggested arrangement, require arbitration among the directors for access to the shared, i.e., global memory; (2) the memory controller 208 of Gaskins is clearly a ***controller*** as shown in FIG. 3 of Gaskins and ***not a network***; (3) the controller 208 of Gaskins does not operate independently of the memory (after all it is the controller for the memory); and, (4) there is nothing in either Martin et al or Gaskins to suggest ***separating*** user data from messages such that the messages used to control the flow of user data pass between one another through a message network so that the passing messages by-pass a global memory, ***such global memory being accessible for data by a plurality of directors such separation thereby removing the very arbitration requirement which would result from the Examiner's suggested arrangmrent***.

More particularly, Applicant wished to make the following points:

1. Applicant has a global memory for storing user data. The global memory is accessible by all directors. Because all directors have access to the global memory for user data there is a requirement for arbitration to decide which one of multiple requesting directors has access to the memory. This arbitration for the memory by the plurality of directors ***reduces system bandwidth. Therefore, the Examiner's position that the use of a memory accessible by a plurality of directors increases bandwidth is not understood.***

2. With applicant's system of FIG. 2 and the prior system in FIG. 1, the control of the data between the host computer and disk drives is by processors in the directors. Thus, it is the plurality of directors that control the flow of data between the host computer and disk drives. The control in the applicant's system of FIG. 2 and the prior system in FIG. 1 is by messages which pass between the directors. In the prior system described in connection with FIG. 1 both the messages and user data went to the global memory. The Applicants recognized that the **bandwidth of the system of FIG. 1 could be increased** by having the message ***BY-PASS*** the global memory as described in FIG. 2. That is, the bandwidth of the system of FIG. 1 was increased because the messaging did not require the arbitration for access to the global memory as the data did for access to such memory. Thus, while the user data continued to pass to the global memory, ***the bandwidth was increased by having the messages BY-PASS the global memory.***

3. Reference is made to the first two paragraphs of the Summary section of the patent applications:

> In accordance with the present invention, a system interface is provided. Such interface includes a plurality of first directors, a plurality of second directors, a data transfer section and a message network. The data transfer section includes a cache memory. ***The cache memory is coupled to the plurality of first and second directors. The messaging network operates independently of the data transfer section and such network is coupled to the plurality of first directors and the plurality of second directors***. The first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the messaging network to facilitate data transfer between first directors and the second directors. The data passes through the

> cache memory in the data transfer section.
>
> With such an arrangement, ***the cache memory*** in the data transfer section ***is not burdened with the task of transferring the director messaging*** but ***rather*** a messaging ***network*** is provided, ***operative independent of the data transfer section,*** for such messaging *thereby* ***increasing the operating bandwidth*** *of the system interface.* (emphasis added)

4. Referring to Martin et al., there is no suggestion of ***separating*** user data from messages such that the messages used to control the flow of user data pass between one another through a message network so that the passing messages by-pass a global memory, ***such global memory being accessible for data by a plurality of directors***. Examiner suggests adding the teaching of Gaskins to Martin et al., and refers to cache controller 208 of Gaskins as a message network. Cache controller 208 is just what it says, it ***is a controller***. ***The cache controller 208 does not pass messages through it between a plurality of directors. Further, the cache memory controller 28 is not operative independently of the data transfer section.***

With regard to Gaskins, reference is made to column 7, lines 29-38:

> Cache controller 208 ***orchestrates*** the transfer of control signals between CPU 202 and bus interface unit 210, and further manages the transfer of data between CPU 202, cache memory 206 and bus interface unit 210. Cache controller 208 partially consists of conventional logic circuitry that allows the cache memory 206 to be read, written, updated, invalidated and flushed. It should be noted that in the preferred form, CPU 202, cache memory 206 and cache controller 208 ***operate concurrently*** to provide maximum sustained performance in the computer system. (emphasis added)

It is first noted that cache controller 208 is clearly a ***controller*** which "***orchestrates*** the transfer " as distinguishes from a network which ***passes messages***; and is it next noted that cache controller 208 partially consists of conventional logic circuitry that allows the cache memory 206 to be read, written, updated, invalidated and flushed. It should be noted that in the preferred form, CPU 202, cache memory 206 and cache controller 208 ***operate concurrently*** and hence the cache controller 208 does not operate independently of the cache memory.

Thus, it is clear that: (1) the memory controller 208 a ***controller*** and ***not a network***; (2) it does not operate independently of the memory (after all it is the controller for the memory); and, (3) there is nothing in either Martin et al or Gaskins to suggest ***separating*** user data from messages such that the messages used to control the flow of user data pass between one another through a message network so that the passing messages by-pass a global memory, ***such global memory being accessible for data by a plurality of directors***.

5. Neither the advantage nor the suggest to ***separate the control messages from the user data*** such that the ***user data goes through the global memory*** while the ***control messages pass between the directors through a message network and BY-PASS the global memory*** is not described or recognized in Martin et al. or Gaskins (U. S. Patent No. 5,903,911) taken either singly or in combination.

6. Neither the advantage nor the suggest to ***operate the message network independently of the data transfer section or global memory are*** described or recognized in Martin et al. or Gaskins (U. S. Patent No. 5,903,911) taken either singly or in combination.

7. Examiner's attention is directed to FIG. 7 of the patent application. As shown therein, each of the director boards 190_1-210_8 has a cross bar switch 320. Each cross bar switch 320 has ***two output/inout ports 325_1 and 325_2***. These BOTH ports are connected to the message network 160. ***More particularly, the message network 160 is made up of a pair of redundant message network BORADS 304_1 and 304_2***. The use of two message network boards connected to all director boards 190_1-210_8 via the two ports ***325_1 and 325_2*** on the cross bar switch 320 is for load balancing of the messages and in case one message network board fails. Applicant seeing nothing like this arrangement in either Martin et al., and or Gaskins taken either singly or in combination.

Notwithstanding the above, and referring to the claims:

Claim 1 points out that the system interface includes:

(a) a plurality of ***first director boards***, each one of the first director boards having:

(i) a plurality of first directors; and

(ii) ***a crossbar switch*** having input/output ports coupled to the first directors on such one of the first director boards and ***a pair of output/input ports***;

(b) a plurality of second director ***boards,*** each one of the second directors boards having:

(i) a plurality of second directors; and

(ii) ***a crossbar switch*** having input/output ports coupled to the second directors on such one of the second director boards and ***a pair of output/input ports***;

(c) a ***data transfer section*** having a cache memory, such ***cache memory being coupled to the plurality of first and second directors;***

(d) a message network, ***operative independently of the data transfer section,*** coupled to ***the pair of output/input ports of each one of the directors boards of the plurality of first director boards and to the pair of output/input ports of each one of the directors boards of the plurality of second director boards***; (emphasis added).

It is respectfully submitted that such an arrangement is not described or suggested in Martin et al. and/or Gaskins taken either singly or in combination.

Claim 8 points out that the system interface includes:

(a) a plurality of first director ***boards*** coupled to host computer/server; each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a ***crossbar switch*** having input/output ports coupled to the first directors on such one of the first director boards and a ***pair of output/input ports***;

(b) a plurality of second ***director boards*** coupled to the bank of disk drives, each one of the second director boards having:

(i) a plurality of second directors; and

(ii) a ***crossbar switch*** having input/output ports coupled to the second directors on such one of the second director boards and ***a pair of output/input ports***;

(c) ***a data transfer section*** having a cache memory, ***such cache memory being coupled to the plurality of first and second directors;***

(d) a message network, ***operative independently of the data transfer section***, coupled to the pair of output/input ports of each one of the directors boards of the plurality of first director boards and to ***the pair of output/input ports*** of each one of the directors boards of the plurality of second director boards; (emphasis added)

It is respectfully submitted that such an arrangement is not described or suggested in Martin et al. and/or Gaskins taken either singly or in combination.

Claim 15 points out that the system interface includes:

(a) a plurality of first director ***boards***, each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a ***crossbar switch*** having input/output ports coupled to the first directors on such one of the first director boards and ***an output/input port;***

(b) a plurality of second ***director boards,*** each one of the second directors boards having:

(i) a plurality of second directors; and

(ii) ***a crossbar switch*** having input/output ports coupled to the second directors on such one of the second director boards and ***an output/input port***;

(c) a ***data transfer section*** having a cache memory, such ***cache memory being coupled to the plurality of first and second directors;***

(d) wherein the ***data transfer section is also coupled to the output/input port of the crossbar switch of each one of the plurality of first director boards and to the output/input port of the crossbar switch of each one of the plurality of second director boards*** a message network, ***operative independently of the data transfer section***; ; (emphasis added)

It is respectfully submitted that such an arrangement is not described or suggested in Martin et al. and/or Gaskins taken either singly or in combination.

Claim 22 points out that the system interface includes:

(a) a plurality of first director ***boards*** coupled to host computer/server; each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a ***crossbar switch*** having input/output ports coupled to the first directors on such one of the first director boards and an ***output/input port***;

(b) a plurality of second director ***boards*** coupled to the bank of disk drives, each one of the second director boards having:

(i) a plurality of second directors; and

(ii) a ***crossbar switch*** having input/output ports coupled to the second directors on such one of the second director boards and ***an output/input port***;

(c) a ***data transfer section*** having a cache memory, such ***cache memory being coupled to the plurality of first and second directors;***

(d) ***wherein the data transfer section is also coupled to the output/input port of the crossbar switch of each one of the plurality of first director boards and to the output/input port of the crossbar switch of each one of the plurality of second director boards;***

(e) a message network, ***operative independently of the data transfer section***; ; (emphasis added)

It is respectfully submitted that such an arrangement is not described or suggested in Martin et al. and/or Gaskins taken either singly or in combination.

Claim 29 points out that the system interface includes:

(a) a plurality of first ***director boards***, each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a ***crossbar switch*** having input/output ports coupled to the first directors on such one of the first director boards and an ***output/input port***;

(b) a plurality of second director ***boards***, each one of the second directors boards having:

(i) a plurality of second directors; and

(ii) a ***crossbar switch*** having input/output ports coupled to the second directors on such one of the second director boards and an ***output/input port***;

(c) ***a data transfer section*** having a cache memory, such ***cache memory being coupled to the plurality of first and second directors;***

(e) ***wherein the data transfer section is also coupled to the output/input port of the crossbar switch of each one of the plurality of first director boards and to the output/input port of the crossbar switch of each one of the plurality of second director boards;***
a message network, operative independently of the data transfer section ; (emphasis added)

It is respectfully submitted that such an arrangement is not described or suggested in Martin et al. and/or Gaskins taken either singly or in combination.

Claim 29 points out that the system interface includes:

(a) a plurality of first director ***boards***, each one of the first director boards having:

(i) a plurality of first directors, each one of the directors having a data port and a message port; and

(ii) a ***crossbar switch*** having input/output ports coupled to the message ports of the first directors on such one of the first director boards and a pair of output/input ports;

(b) a plurality of second ***director boards***, each one of the second directors boards having:

(i) a plurality of second directors, each one of the directors having a data

port and a message port; and

(ii) ***a crossbar switch*** having input/output ports coupled to the message ports of the second directors on such one of the second director boards and ***a pair of output/input ports;***

(c) ***a data transfer section*** having a cache memory, ***such cache memory being coupled to the data ports of the plurality of first and second directors;***

(d) ***a message network, coupled to the pair of output/input ports of each one of the directors boards of the plurality of first director boards and to the pair of output/input ports of each one of the directors boards of the plurality of second director boards;***
(emphasis added)

It is respectfully submitted that such an arrangement is not described or suggested in Martin et al. and/or Gaskins taken either singly or in combination.

Claim 31 points out that the system interface includes:

(a) a plurality of first director ***boards***, each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a ***crossbar switch*** having input/output ports coupled to the first directors on such one of the first director boards and ***a pair of output/input ports***;

(b) a plurality of second ***director boards***, each one of the second directors boards having:

(i) a plurality of second directors; and

(ii) a ***crossbar switch*** having input/output ports coupled to the second directors on such one of the second director boards and a ***pair of output/input ports***;

(c) ***a data transfer section*** having a cache memory, ***such cache memory being coupled to the plurality of first and second directors;***

(d) ***a message network, operative independently of the data transfer section, coupled to the pair of output/input ports of each one of the directors boards of the plurality***

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of first director boards and to the pair of output/input ports of each one of the directors boards of the plurality of second director boards; (emphasis added)

It is respectfully submitted that such an arrangement is not described or suggested in Martin et al. and/or Gaskins taken either singly or in combination.

As noted above, the Examiner's attention is directed to FIG. 7 of the patent application. As shown therein, each of the director boards 190_1-210_8 has a cross bar switch 320. Each cross bar switch 320 has ***two output/inout ports 325_1 and 325_2***. These BOTH ports are connected to the message network 160. ***More particularly, the message network 160 is made up of a pair of redundant message network BORADS 304_1 and 304_2***. The use of two message network boards connected to all director boards 190_1-210_8 via the two ports ***325_1 and 325_2*** on the cross bar switch 320 is for load balancing of the messages and in case one message network board fails. Applicant seeing nothing like this arrangement in either Martin et al., and or Gaskins taken either singly or in combination. ,

Thus, Applicant respectfully disagrees with the rejection of the claim 1-31 under 35 USC 103(a) as being unpatentable over Martin et al. (U. S. Patent No. 5,214,768) in view of Gaskins (U. S. Patent No. 5,903,911).

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 05-0889.

Respectfully submitted,

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Date

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